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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,510	03/15/2004	Tien-I Bao	TSM03-0927	9453

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,510	BAO ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *1-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 03/15/2004 is acceptable.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "said thin stop layer is multilayered" of claims 5, 12, and 32 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Election/ Restriction

3. Applicant's election of Invention II, claims 24-43, in the reply filed on 03/01/2005, is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

4. Claims 1-23 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 03/01/2005 as noted above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 24-25 and 28-29** are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. U.S. Patent 6,417,090 (the '090 patent).

The '090 patent discloses in Figures 2-8 and respective portions of the specification a semiconductor device and a method of fabricating thereof as claimed.

Referring to **claim 24,** the '090 patent discloses a method for processing a semiconductor structure defining a metallization layer (32) which results in said metallization layer being substantially free of damage comprising the steps of:

capping a top surface of said semiconductor structure that defines said metallization layer with a thin stop layer (34, "thin" is interpreted broadly);

forming a layer (36, column 5, lines 19-20) of dielectric over said layer of thin stop, said layer of dielectric defining at least one area (40, Fig. 5) where said thin stop layer (34) is exposed; and

removing said exposed thin stop layer to expose a top surface of said metallization layer (32, Fig. 6) which is substantially free of damage (Abstract: "Following the etching of the dielectric layer, which stops on the etch stop layer, the etch stop layer is then etched with a chemistry that does not damage the underlying copper in the metal interconnect layer").

In re claim 25, the '090 patent further discloses that said step of forming a layer of dielectric comprises forming a patterned layer of dielectric according to a patterned layer of resist (38), said pattered layer of dielectric defining a layout for an upper layer of metallization (42, Fig. 8), and said step of removing further comprises removing said patterned layer of resist (note that numerical references in Figs. 7 and 8 of the '090 patent are mislabeled).

Referring to **claim 28**, the reference further discloses that the step of filling said layout etched in said dielectric layer with a conductive metal, such as copper (42, column 6, lines 1-4).

Referring to **claim 29**, the reference further discloses that said thin stop layer is an organic material (HSQ or SILK, column 5, lines 5-10; and see U.S. Patent Application Publication 20030129844 by Wang et al., paragraph [0006], for a statement that HSQ and SILK, disclosed by the '090 patent, are organic materials).

6. **Claims 24-25, 28, and 30** are rejected under 35 U.S.C. 102(b) as being anticipated by Tang U.S. Patent 6,117,793 (the '793 patent).

The '793 patent discloses in Figures 1-9 and respective portions of the specification a semiconductor device and a method of fabricating thereof as claimed.

Referring to **claim 24,** the '793 patent discloses a method for processing a semiconductor structure defining a metallization layer (104/106, barrier layer 106 being optional, column 4, first paragraph) which results in said metallization layer being substantially free of damage comprising the steps of:

capping a top surface of said semiconductor structure that defines said metallization layer with a thin stop layer (108, also column 4, first paragraph; and "thin" is interpreted broadly);

forming a layer (116, column 4, second paragraph) of dielectric over said layer of thin stop, said layer of dielectric defining at least one area (124, Fig. 7) where said thin stop layer (108) is exposed; and

removing said exposed thin stop layer to expose a top surface of said metallization layer (104/106, Fig. 8) which is substantially free of damage (column 2, lines 38: "Thus, it can be appreciated that it would be advantageous to develop a technique to form a via which prevents the formation of metal polymer residues and allows for removal of oxide polymer residues from

the via without substantial damage to the metal-containing trace or pad while using commercially-available, widely-practiced semiconductor device fabrication techniques").

In re claim 25, the '793 patent further discloses that said step of forming a layer of dielectric comprises forming a patterned layer of dielectric according to a patterned layer of resist (118), said pattered layer of dielectric defining a layout for an upper layer of metallization (132, Fig. 9), and said step of removing further comprises removing said patterned layer of resist.

Referring to **claim 28**, the reference further discloses that the step of filling said layout etched in said dielectric layer with a conductive metal, such as copper (column 4, lines 57-65).

Referring to **claim 30**, the reference further discloses that said thin stop layer (108) contains a metal ("tungsten", column 4, lines 3-5).

Claim Rejections § 102 & § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 24-34 and 42-43** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ruelke et al. U.S. Patent Application Publication 20040084680 (the '680 publication).

The '547 publication discloses in the Figs. 2's and respective portions of the specification a method for processing a semiconductor structure as claimed or substantially as claimed.

Referring to **claim 24,** the '680 publication discloses a method for processing a semiconductor structure defining a metallization layer (203, paragraph [0033]) which results in or may result in said metallization layer being substantially free of damage comprising the steps of:

capping a top surface of said semiconductor structure that defines said metallization layer with a thin stop layer (250, paragraph [0033]);

forming a layer (206) of dielectric over said layer of thin stop, said layer of dielectric defining at least one area (211, Fig. 2g and paragraph [0046]) where (a portion of) said thin stop layer (250) is exposed (note that in forming area 211, which is by etching through dielectric 206 using mask 209, which process is similar to the present invention, there is no guarantee that the (complete) thin stop layer 250 is exposed; a portion 255 of the thin stop layer 250 being exposed is a more likely scenario); and

removing said exposed thin stop layer to expose a top surface of said metallization layer (203, Fig. 2i) which is substantially or appears to be substantially free of damage (note that although the reference does not appear to disclose the limitation "substantially free of damage" as claimed, the materials, process, and the thickness for the thin stop layer, as will be apparent in the following paragraphs, are the same as claimed, and therefore would possess or appear to possess the missing limitation).

In re claim 25, the '680 publication further discloses that said step of forming a layer of dielectric comprises forming a patterned layer of dielectric according to a patterned layer of resist (209), said pattered layer of dielectric defining a layout for an upper layer of metallization

(219, Fig. 2j), and said step of removing further comprises removing said patterned layer of resist.

Referring to **claims 42 and 26-27**, and using the same references, citations, and interpretations as detailed above for claim 24 where applicable, the reference discloses a method of forming the layout for an upper level of metallization (219) in a semiconductor that appears to have reduced damage to a lower level of metallization (203) comprising the steps of:

providing a substrate (201) having a surface, said surface including a top surface of said lower level of metallization;

capping said lower level of metallization with a stop layer deposited to a thickness of less than 300 angstroms (10-100 nm, paragraph [0035], and note that although the passage does not exactly disclose "less than 300 angstroms", the reference discloses a "required thickness", which is interpreted to be within the skill of an ordinary artisan in the art to chose, in the range of 10-100 nm, which range overlaps the claimed thickness) over said surface;

forming a patterned layer of dielectric over said etch stop layer according to a patterned layer of resist on said dielectric layer, said patterned dielectric layer defining said layout for an upper level of metallization, and said layout including at least one area where said etch stop layer is exposed; and

removing said patterned resist and said exposed etch stop layer to expose, substantially damage free, a portion of said top surface of said lower level of metallization.

Referring to **claims 43 and 28**, and using the same references, citations, and interpretations as detailed above for claims 24 and 42 where applicable, the reference discloses a

method of forming an upper level of metallization in a semiconductor device with reduced damage to a lower level of metallization comprising the steps of:

providing a substrate having a top surface, said top surface defining said lower level of metallization;

capping said lower level of metallization with a stop layer deposited to a thickness of less than 300 angstroms over said top surface;

depositing a layer of inter-metal dielectric (IMD) (206) over said stop layer;

depositing and patterning a layer of resist to define a patterned mask over said layer of a IMD;

etching said layer of IMD to remove material according to said mask, said removed material defining the layout for an upper level of metallization, and said layout including at least one area where said layer of IMD is completely etched through to expose said stop layer;

removing said patterned resist and said exposed stop layer; and

filling said layout etched in said IMD layer with metal (219, copper, paragraph [0050]) to form said upper layer of metallization.

Referring to **claim 31**, the material list of the reference (silicon carbide or SiC, SiCN, paragraph [0033]) for the thin stop layer meets the requirement of the claimed Markush group.

Referring to **claim 32**, the reference further discloses that said thin stop layer is multilayered (250a and 250b).

Referring to **claim 33**, the process for forming the thin stop layer of the reference (CVD, paragraph [0035]) meets the requirement of the claimed Markush group, and the claimed temperature of **claim 34** appears to be inherent in the reference because the reference does not

disclose that the thin stop layer is formed by a high temperature process, which is above 500 degree C.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 35-41** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '680 publication for being obvious.

The '680 publication discloses a method for processing a semiconductor structure defining a metallization layer as claimed or substantially as claimed and as detailed above. The reference further discloses forming a trench (no number) in dielectric 204, and forming a barrier layer (in re claim 36 and paragraph [0033]). However, the reference fails to disclose a seed layer. However, the use of a seed layer in forming a metalization layer is widely known in the art for the advantage of, as the name suggests, forming a template upon which the metallization layer is formed. See, for example, Morrow et al. U.S. Patent Application Publication 20040058547, paragraph [0015]. Since the modification including a seed layer is known in the art, the change to include such a layer would have been obvious to one of ordinary skill in the art at the time the invention was made and therefore would not be patentable.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
March 25, 2005